FACULTY PROFILE

1.	**Name**	:	**PradeepKumar S K**	
2.	**Date of Birth**	:	**13 Nov 1987**	
3.	**Highest Qualification.**	:	**M.Tech**	
	Specialization	:	**VLSI Design and Embedded System**	
4.	**Academic Performance**	:		

(High School to Highest Qualifications)

Qualifications	Board / IIT / University	Institute and place where studied	Year of passing	Class & % marks
SSLC	KSEE Board	Govt Boys Junior College, Tiptur	2003	FC/80.35
PUC /10+2/Dip	KDPU Education	DVS Composite PU College, Shimoga	2005	FC/71.78
UG Degree	VTU, Belgaum	KIT, Tiptur	2009	FC/63.00
PG Degree	VTU, Belgaum	CMR Institute of Technology, Bangalore	2011	FC/69.19

5.	**Date of Joining**	:	**19 Sep 2011**
6.	**Status as on date of Joining**	:	**Lecturer**
7.	**Salary as on date of Joining**	:	**Rs.20,450/-**
8.	**Present Status**	:	**Assistant Professor**
9.	**Salary as on date**	:	**Rs.32,656/-**
10.	**Number of promotions since date of joining**	:	**01**

11. Achievements since date of joining:

a) Faculty Development / QIP	:	**15**
b) Research & Development	:	**01**
c) No. of Publication (List)	:	**02**
d) Presentation Award	:	**--**
e) Books / Monograph (List)	:	**--**
f) Conference Seminars (List)	:	**International – 04, National - 02**
g) Extra curricular activities*	:	**--**
h) Administrative Work	:	**--**

FD-Faculty Development, R&D-Research and Development

Note: *Activities listing, follow University classification.

Publication Date	Name, title of the Paper, N/I Journal, pages, year, also list here the Books and Monographs	
CAY 2021-22	---	
CAYm1 20-21	---	
CAYm2 19-20	---	
CAYm3 18-19	---	
CAYm4 17-18	**"*Fewer cost and superior functioning architecture of VSLI premeditated with Multiplication of Montgomery*",** International Journal of VLSI & Signal Processing DOI: 10.14445/23942584/IJVSP-V4I3P102 SSRG - IJVSP Journal Volume 4 Issue 2	International Journal

CAYm5 16-17	***"High Speed and Resource Efficient Systolic Architecture for Matrix Multiplication using FPGA"*** GRD Journals- Global Research and Development Journal for Engineering | Volume 1 | Issue 5 | April 2016 ISSN: 2455-5703	International Journal
CAYm6 15-16	---	
CAYm7 14-15	---	
CAYm8 13-14	---	
CAYm9 12-13	---	
CAYm10 11-12	---	
Conference / Seminar/W/s	**Name, title of the paper, Conference / Seminar, venue and date**	
CAY 2021-22	**6-Day** online FDP on " ***Current Era – A Technology driven Digital Transformation in Industry 4.0***" from 30/08/2021 to 04/09/2021, organized by Department of ISE, SJB Institute of Technology, Bengaluru.	FDP
	5-Day FDP on "***Digital VLSI Design and Verification***" organized by Department of ECE, Bangalore Institute of Technology in association with Entuple Technologies and IEEE-BIT CAS from 23rd to 27th August 2021.	FDP
	One Week Online Faculty Development Program on "***Introduction to Microchip FPGA"*** from 19th to 23rd July 2021, organized by Department of Electronics & Communication Engineering, Bapuji Institute of Engineering and Technology, Davangere in association with Tecnomic Components Pvt. Ltd. Bengaluru, ISTE Faculty Chapter BIET and IETE Shivamogga Center.	FDP
	One Week Online Faculty Development Program on "***Data Analytics Using Artificial Intelligence & Machine Learning"*** held during April 12th -17th, 2021 organized by Department of ECE, HKBK College of Engineering, Nagawara, Bengaluru.	FDP
CAYm1 20-21	**8 Week** Winter Online ***IP Research Internship*** from **Sep to Nov 2020** organized by VLSI System Design Corporation. **IP Designed:** *"Design of 4KB Static RAM 1.8V (access time <2.5ns) using OpenRAM and Sky130 node"* https://github.com/pradeepsk13/vsdsram_sky130_1.8V	Research Internship
	5-day workshop on **"*RISC-V based SoC design using open-source*"**, an online cloud based workshop conducted by VSD from 27 - 31 May 2020.	Workshop
CAYm2 19-20	***"CAF Technique in Position Recognition for Wireless Application"***, 2020 International Conference on Recent Trends on Electronics, Information, Communication & Technology (RTEICT), 12-13 Nov. 2020, Bangalore, India. pp. 337-342, doi: 10.1109/RTEICT49044.2020.9315677.	International Conference
CAYm3 18-19	Participated in one day workshop on "Learning Effective Document Writing using Latex" at KIT, Tiptur, on 15th April 2019	Workshop
CAYm4 17-18	***"Less cost and superior operational architecture of VSLI designed with Multiplication of Montgomery"***.International Conference on Wearable Technologies , ICOWT-2017, Bengaluru, Karnataka, India,22nd to 23rd June 2017.	International Conference
	"***Advances in Image Processing and Computer Vision Applications using Python and OpenCV"*** at K.I.T.,Tiptur, from 11th to 23rd December 2017.	FDP
CAYm5 16-17	***"ASIC Realization and Performance Evaluation of 64×64 Bit High speed Multiplier in CMOS 45nm using Wallace Tree"***. IEEE International Conference On Recent Trends In Electronics Information Communication Technology, Bengaluru, Karnataka, India, May 19-20, 2017.	International Conference
	National Conference on Emerging Trends in Engineering Science and Management (NCESM-2016) held on **23rd to 24th March 2016** on paper titled **"*Systolic Architecture for integer point matrix multiplication using FPGA***", at SIET, Tumakuru.	National Conference

CAYm6 15-16	Workshop on **"*Analog and Digital IC Design using Cadence Tool*"** at KIT, Tiptur, from 5th to 6th April 2016	Workshop
	National Conference on Advancements in information Technology May 5th and 6th, 2015 on paper Titled," ***2D FIR filter using an improved addition and multiplication Techniques*"**, at JSSATE, Bangalore.	National Conference
	"*Analog, Power, Embedded Systems and Wireless (IoT) hands on workshop*" conducted jointly by Texas Instruments, Bangalore and STEPS Knowledge Service Pvt. Ltd., Coimbatore held during 11th to 14th July 2016 at REVA University, Bangalore	FDP
	International conference***," 2D FIR filter using an improved addition and multiplication Techniques***", in 2nd International conference ICRTSIV on 15th, 16th May 2015, Don Bosco Institute of Technology, Bangalore.	International Conference
CAYm7 14-15	Two Week ISTE Workshop on ***"Signals and Systems***" conducted by IIT Kharagpur from 2nd to 12th Jan 2014, at Manipal Institute of Technology, Manipal.	Workshop
	"***Analog and Digital VLSI Design using Cadence tools***", 28th to 30th April 2014, RIT, Hassan	Workshop
CAYm8 13-14	"***Feel Teacher ",*** Learning and Development intervention, from 28th to 30th Jan 2012, at KIT, Tiptur.	Workshop
	"VLSI design Lab using Open source ", 24th, 25th July 2013, MSCE, Bangalore.	Workshop
CAYm9 12-13	"***IEEE Explore digital Library User Awareness Programme***", Nov 7th 2012, at KIT, Tiptur.	Workshop
CAYm10 11-12	One Week CEP Short Term Course entitled ***"FPGA Prototyping in VERILOG,***" IIT Kharagpur. June 24th - 30th , 2012.	STC

Co & Extra-curricular	**Participation in Co and extracurricular activities (member of respective committees / office bearer / Group leader etc.)**	**Prizes / Awards**
	NIL	

12. Experience / Service before Joining:

Sl. No.	**Name & Address of Organization / Institution**	**Post Held / Designation**	**Duration of service**		**Experience Y/M**			
			From	**To**	**T**	**R**	**Ind.**	**Total**
01	LRDE, DRDO Bengaluru	Trainee Engineer	June 2010	May 2011		10M		10M

T – Teaching, R – Research, Ind. - Industry

13. Memberships of Professional Bodies:

Sl. No.	**Name & Address of Organization / Institution**	**Date & Year of Registration**	**Membership Number**
1	MISTE	2014	LM96709

Signature

(PRADEEPKUMAR S K)